NOIDA INTERNATIONAL UNIVERSITY
GAUTAM BUDH NAGAR, UP

EVALUATION SCHEME & SYLLABUS

FOR

MASTER OF TECHNOLOGY

In

VLSI AND EMBEDDED SYSTEMS (WEEKEND)

AS PER
AICTE MODEL CURRICULUM
[Effective from the Session: 2019-20]

Program Outcomes (POs)

Students will be able to

1. Apply the knowledge of science, mathematics, and engineering principles for developing problem solving attitude.

2. Identify, formulate and solve engineering problems in the broad areas like System Design using VLSI and Embedded Platforms and tools, Semiconductor Technologies, Applications in Signal Processing, Machine Vision and Communication Networks.

3. Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor-planning, Place and route, Layout editors, RTL schematic, Platform specific EDA sets, MATLAB.

4. Design and conduct experiments, analyze and interpret data, imbibe programming skills for development of simulation experiments.

5. Function as a member of a multidisciplinary team with sense of ethics, integrity and social responsibility

Semester-1								
Paper code	**Subject**	**L**	**T**	**P**	**Marks(ISA)**	**Marks(ESE)**	**Total**	**Credit**
VPCT1	RTL Simulation and Synthesis with PLDs	3	0	0	40	60	100	3
VPCT2	Microcontrollers and Programmable Digital Signal Processors	3	0	0	40	60	100	3
VPCL1	RTL Simulation and Synthesis with PLDs Lab	0	0	4	40	60	100	2
VPCL2	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4	40	60	100	2
Total							**400**	**10**

Semester-2								
Paper code	**Subject**	**L**	**T**	**P**	**Marks(ISA)**	**Marks(ESE)**	**Total**	**Credit**
VPCT3	Analog and Digital CMOS VLSI Design	3	0	0	40	60	100	3
VPCT4	VLSI Design Verification and Testing	3	0	0	40	60	100	3
VPCL3	Analog and Digital CMOS VLSI Design Lab	0	0	4	40	60	100	2
VPCL4	VLSI Design Verification and Testing Lab	0	0	4	40	60	100	2
Total							**400**	**10**

Semester-3								
Paper code	**Subject**	**L**	**T**	**P**	**Marks(ISA)**	**Marks(ESE)**	**Total**	**Credit**
VPE1x	Program Elective-1 (1) Digital Signal and Image Processing (2) Programming Languages for Embedded Software (3) VLSI signal processing	3	0	0	40	60	100	3
VPE2x	Program Elective-2 (1) Parallel Processing (2) System Design with Embedded Linux (3) CAD of Digital System	3	0	0	40	60	100	3
MTC01	Research Methodology and IPR	2	0	0	40	60	100	2
	Audit Course-1	2	0	0	40	60	100	0
Total							**400**	**8**

Semester-4								
Paper code	**Subject**	**L**	**T**	**P**	**Marks(ISA)**	**Marks(ESE)**	**Total**	**Credit**
VPE3x	Program Elective-3 (1) Memory Technologies (2) SoC Design (3) Low power VLSI Design	3	0	0	40	60	100	3
VPE4x	Program Elective-4 (1) Communication Buses and Interfaces (2) Network Security and Cryptography (3) Physical design automation	3	0	0	40	60	100	3
	Audit Course-2	2	0	0	40	60	100	0
MTC02	Mini Project with Seminar	0	0	4	100	0	100	2
Total							**400**	**8**

Audit course 1 & 2

MAC01. English for Research Paper Writing
MAC02. Disaster Management
MAC03. Sanskrit for Technical Knowledge
MAC04. Value Education
MAC05. Constitution of India
MAC06. Pedagogy Studies
MAC07. Stress Management by Yoga
MAC08. Personality Development through Life Enlightenment Skills

Semester-5								
Paper code	**Subject**	**L**	**T**	**P**	**Marks(ISA)**	**Marks(ESE)**	**Total**	**Credit**
VPE5x	Program Elective-5 (1) Communication Network (2) Selected Topics in Mathematics (3) Nano materials and Nanotechnology	3	0	0	40	60	100	3
	Open Elective	3	0	0	40	60	100	3
MTC03	Dissertation Phase-1	0	0	20	500	0	500	10
Total							**700**	**16**

Semester-6								
Paper code	**Subject**	**L**	**T**	**P**	**Marks(ISA)**	**Marks(ESE)**	**Total**	**Credit**
MTC04	Dissertation Phase-2	0	0	32	500	200	700	16
Total							**700**	**16**

GRAND TOTAL	**3000**	**68**

Open Elective

MOE01. Business Analytics
MOE02. Industrial Safety
MOE03. Operations Research
MOE04. Cost Management of Engineering Projects
MOE05. Composite Materials
MOE06. Waste to Energy

Course Code : VPCT1 **Course Name: RTL Simulation & Synthesis with PLDs**
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective :

To describe both simple and complex RTL design scenarios using VHDL/verilog. It gives practical information on the issues in ASIC prototyping using FPGAs, design challenges and how to overcome practical issues and concerns.

Course Description:

With this course the students will able to understand the concept of simulation & synthesis of complex circuits using VHDL/VERILOG.

Course Contents :

Unit1

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

Unit 2

Design entry by Verilog/VHDL/FSM, Verilog AMS.

Unit 3

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

Unit 4

Design for performance, Low power VLSI design techniques. Design for testability.

Unit 5

IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping

Unit 6

Case studies and Speed issues.

Course Learning Outcomes(CLOs) :

CO1: Describe Finite State Machines and comprehend concepts of clock related issues.

CO2: Model digital circuits using Verilog and understand the concepts of analog and mixed signal Systems design using Verilog AMS.

CO3: Outline the concepts of different design flows in VLSI.

CO4: Illustrate different low power latches and Flip-flops.

CO5: Explain the concepts of IP cores and Prototyping.

Text books :

- Richard S. Sandige, Modern Digital Design , MGH, International Editions,1990
- T. R. Padmanabhan and B. F.V.G. Bala Tripura Sundari, Design through Verilog HDL , WSE, IEEE Press, 2004.
- Zeidman, Bob. Designing with FPGAS and CPLDS . CRC Press, 2002.

- KiatSeng Yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/Bi CMOS ULSI Low Voltage Low Power , Pearson Education Asia 1st Indian reprint, 2002.
- Doug Amos, Austin Lesea, Rene Richter, FPGA based prototyping methodology manual , Xilinx.

Reference books :

- Palnitkar, Samir. Verilog HDL: a guide to digital design and synthesis . Pearson Education India, 2003.
- Givone, Donald D. Digital principles and design . Palgrave Macmillan, 2003.
- Roth, Charles H. Digital systems design using VHDL . Wadsworth Publ. Co., 1998.

Online links for study & reference materials :

http://smdpc2sd.gov.in/downloads/IEP/IEP%208/24-02-18%20Rejender%20pratap.pdf
https://inst.eecs.berkeley.edu/~cs150/sp02/useful_files/Synthesis_Simulation_Design_Guide.pdf

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

CourseCode :VPCT2 C**ourseName :**Microcontrollers & Programmable DSPs
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective :

The course should enable the students to:

- Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- Identify and characterize architecture of Programmable DSP Processors
- Develop small applications by utilizing the ARM processor core and DSP processor based platform

Course Description :

In this course students will understanding the ARM Cortex-M3 processor: Applications, Programming model, Operation modes, Exceptions and Interrupts,the Instruction Set etc. they will understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, LPC 17xx microcontroller. They will study the features of ADC, UART and other serial interfaces. then they will understand the Introduction to TI DSP processor family, architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. And the Code Composer Studio for application development for digital signal processing, on chip peripherals, Processor benchmarking.

Course Contents :

Unit 1

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

Unit 2

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

Unit 3

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

Unit 4

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

Unit 5

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations

Unit 6

Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking

Course Learning Outcomes(CLOs) :

At the end of the course, students will demonstrate the ability to:

- CO 1: Analyze the characteristics of ARM Cortex-M3 processor.
- CO 2: Understand the various Exceptions and Interrupts in Cortex-M3 processor.
- CO 3: Study the features of LPC 17xx microcontrollers based on Cortex-M3 processor.
- CO 4: Identify and analyze the characteristics Programmable DSP Processors.
- CO 5: Understand the TMS320C6000 series DSP Processor architectures.

Text books :

- Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
- Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH , 2nd Edition

Reference books :

- Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication
- Steve furber, "ARM System-on-Chip Architecture", Pearson Education
- Frank Vahid and Tony Givargis, "Embedded System Design", Wiley

Online links for study & reference materials :

www.arm.com ,www.nxp.com, www.ti.com

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

RTL Simulation and Synthesis with PLDs Lab

Teaching Scheme **Paper Code: VPCL1**

Lectures:4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
- Use EDA tools like Cadence, Mentor Graphics and Xilinx.

List of Experiments:

1) Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2) Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3) Vending machines - Traffic Light controller, ATM, elevator control.
4) PCI Bus & arbiter and downloading on FPGA.
5) UART/ USART implementation in Verilog.
6) Realization of single port SRAM in Verilog.
7) Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8) Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Microcontrollers and Programmable Digital Signal Processors Lab

Teaching Scheme **Paper Code: VPCL2**

Lectures: 4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
- Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

Course Code: VPCT3 **Course Name : Analog and Digital CMOS VLSI Design**
Course Credit: **Total Contact Hour:** 40hr

Course Objective :

- To understand the construction, operation and mathematical models of MOSFETs.
- To analyze and design single stage and multistage amplifiers at low frequencies.
- To study and analyze different current mirrors used to bias IC amplifiers.
- To understand the frequency response of amplifier designed in integrated circuits.
- To understand the principles of operation of different feedback topologies.
- To understand different specifications and topologies related to operational amplifiers.

Course Description :

This course is focused on applications of digital CMOS circuits and to understand the fabrication process of CMOS technology. Design of combinational and sequential circuits and implementation of the circuits with the help of FPGA, CPLD and some other form of devices is discussed. This course introduces the student, to the fundamentals of MOS device physics and building blocks of analog integrated circuit design.

Course Contents :

Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process

Digital CMOS Design:

Unit 1

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models.

Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

Unit 2

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.

Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Unit 3

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit.

Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design:

Unit 4

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models.

Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Unit 5

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

Unit 6

Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
- Connect the individual gates to form the building blocks of a system.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

Text books :

- J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
- Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
- Behzad Razavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Reference books :

- Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
- R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
- Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rd Edition.
- Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Online links for study & reference materials :

https://nptel.ac.in/content/storage2/courses/117101105/downloads/L1.pdf
https://nptel.ac.in/courses/117/101/117101105/

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code : VPCT4 **Course Name : VLSI Design Verification and Testing**
Course Credit: **Total Contact Hour:** 40hr

Course Objective :

In this course the students will learn testing and verification in VLSI design process, ATPG concepts for combinational and sequential circuits.

Course Description :

The student will learn to analyse the use of procedural statements and routines in testbench design with system verilog. And will also learn to interface a system verilog testbench with system C.

Course Contents :

Unit 1

Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

Unit 2

Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

Unit 3

Procedural statements and routines: Procedural statements, tasks, functions and void functions, routine arguments, returning from a routine, local data storage, time values

Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Unit 4

SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench.

Unit 5

Randomization: Introduction, What to randomize, Randomization in System Verilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre-randomize and post-randomize functions,

Unit 6

Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- Familiarity of Front end design and verification techniques and create reusable test environments.
- Verify increasingly complex designs more efficiently and effectively.
- Use EDA tools like Cadence, Mentor Graphics.

Text books :

- Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
- M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers

Reference books :

- Bushnell, M. and Agrawal, V.D., Essentials of Electronic Testing for Digital, Memory and MixedSignal VLSI Circuits, Kluwer Academic (2000).
- Rashinkar, P., Paterson and Singh, L., System-on-a-Chip Verification-Methodology and Techniques, Kluwer Academic (2001)
- Abramovici, M., Breuer, M. A. and Friedman, A.D., Digital Systems Testing and Testable Design, Jaico Publishing House (2001).
- Kropf, T., Introduction to Formal Hardware Verification, Springer Verlag(1999).

Online links for study & reference materials :

- System Verilog website – www.systemverilog.org
- http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
- General reuse information and resources www.design-reuse.com
- OVM, UVM (on top of SV) www.verificationacademy.com
- Verification IP resources
- http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
- http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Analog and Digital CMOS VLSI Design Lab

Teaching Scheme **Paper Code: VPCL3**

Lab work : 4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Design digital and analog Circuit using CMOS.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

List of Experiments:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
    a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
    b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
    c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
    d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
    e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV
    To extract Vth use the following procedure.
        i. Plot gm vs VGS using NGSPICE and obtain peak gm point.
        ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.
        iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
    f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.

    Tabulate your result according to technologies and comment on it.

2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
    a) Perform the following
        i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
        ii. Plot VTC for CMOS inverter with varying VDD.
        iii. Plot VTC for CMOS inverter with varying device ratio.
    b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)
    c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)
3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4) Perform the following
    a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13um process.
    b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.
        i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.
        ii. Calculate input bias voltage if bias current=50uA.
        iii. Use Ngspice and obtain the bias current. Compare its value with 50uA.
        iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).
        v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
        vi. Use Ngspice to determine input voltage range of the amplifier
5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
        i. Draw the schematic of op-amp macro model.
        ii. Draw the schematic of INA.
        iii. Obtain parameters of the op-amp macro model such that
            a. low-frequency voltage gain = 5x104,
            b. unity gain BW (fu) = 500KHz,
            c. input capacitance=0.2pF,
            d. output resistance =_,
            e. CMRR=120dB
        iv. Draw schematic diagram of CMRR simulation setup.
        v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
        vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
        vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.
6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.
    a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three

cascaded minimum sized inverters. Use M1 as interconnect line between inverters.

b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.
d) Use interconnect length obtained and connect the second and third inverter.

Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’.

VLSI Design Verification and Testing Lab

Teaching Scheme **Paper Code: VPCL4**

Lectures: 4 hrs/week

Course Outcomes:

At the end of the laboratory work, students will be able to:

- Verify increasingly complex designs more efficiently and effectively.
- Use EDA tools like Cadence, Mentor Graphics.

List of Assignments:

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

Course Code: VPE11 **Course Name: Digital Signal & Image Processing**
Course Credit: 03 **Total Contact Hour:** 40hr

Course Objective:

- Recall and summarize the digital image fundamentals and to be exposed to basic image processing techniques.
- Be familiar with image segmentation and compression techniques.
- Illustrate the representation of color images in the form of features.

Course Description:

This course provides an introduction to basic concepts, methodologies and algorithms of digital image processing focusing on the following two major problems concerned with digital images: (1) image enhancement and restoration for easier interpretation of images, and (2) image analysis and object recognition. Some advanced image processing techniques (e.g., wavelet and multi resolution processing) will also be studied in this course. The primary goal of this course is to lay a solid foundation for students to study advanced image analysis topics such as computer vision systems, biomedical image analysis, and multimedia processing & retrieval.

Course Contents:

Unit 1

Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.

Unit 2

Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation.

Unit 3

Fixed point implementation of filters – challenges and techniques.

Unit 4

Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – JPEG and JPEG 2000.

Unit 5

Color Image processing – Handling multiple planes, computational challenges.

Unit 6

VLSI architectures for implementation of Image Processing algorithms, Pipelining.

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- Analyze discrete-time signals and systems in various domains
- Design and implement filters using fixed point arithmetic targeted for embedded platforms
- Compare algorithmic and computational complexities in processing and coding digital images.

Text books:

- J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
- Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition.

Reference books:

- S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006
- A. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
- KeshabParhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India

Online links for study & reference materials:

https://nptel.ac.in/courses/106/105/106105032/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code : VPE12 Course Name : Programming Languages for Embedded Software
Course Credit:3 Total Contact Hour: 40hr

Course Objective :

- This subject is framed to set the required background in embedded system concepts, Fundamentals of Linux OS and 'C' language for the rest of the modules.
- It aims at familiarizing the students in embedded concepts and programming in 'C'. This module covers the advanced topics in 'C' such as Memory management, Pointers, Data structures which are of high relevance in embedded software is considered in depth.
- The syllabus also covers the topic 'scripting languages for embedded systems'.

Course Description :

In this course student will learn the syntax and semantics, principles of the C language for embedded programming, how to debug a C program on a target device, how to access memory-mapped peripherals using C, interrupt handlers etc.

Course Contents :

Unit 1

Embedded 'C' Programming: Bitwise operations, Dynamic memory allocation, OS services, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods (Waterfall, Agile)

Unit 2

Object Oriented Programming: Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

Unit 3

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

Unit 4

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

Unit 5

Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.

Unit 6

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- CLO-1 : Write an embedded C application of moderate complexity.
- CLO-2 : Develop and analyze algorithms in C++.
- CLO-3 :Differentiate interpreted languages from compiled languages.
- CLO-4:Get knowledge in Embedded OS (Linux) fundamentals

Text books :

- Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008

Reference books :

- Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011
- A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
- Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
- Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005

Online links for study & reference materials :

https://nptel.ac.in/courses/117/106/117106112/
https://www.youtube.com/watch?v=IY4xrpJQwOY

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code : VPE13 **Course Name :** VLSI signal processing
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective :

- To make an in depth study of DSP structures amenable to VLSI implementation.
- To enable students to design VLSI system with high speed and low power.
- To make the students to implement DSP algorithm in an optimized method.

Course Description :

Digital signal processing (DSP) has emerged over the last two decades as the single most key component in all electronic applications. This course aims at providing a comprehensive coverage of some of the important techniques for designing efficient VLSI architectures for DSP. Towards this, architectural optimization at various levels will be considered. The course may also be used as a reference by industrial professionals interested in VLSI design of signal processing and communication systems.

Course Contents :

Unit 1

Introduction to DSP systems, Pipelined and parallel processing.

Unit 2

Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

Unit 3

Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise.

Unit 4

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.

Unit 5

Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.

Unit 6

Programmable digit signal processors.

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- CO1:Acquired knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
- CO2:Ability to acquire knowledge about retiming techniques, folding and register minimization path problems.
- CO3:Ability to have knowledge about algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters.
- CO4:Acquired knowledge about finite word-length effects and round off noise computation in DSP systems.

Text books :

- S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985

Reference books :

- Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley, Inter Science, 1999.
- Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994

Online links for study & reference materials :

https://nptel.ac.in/courses/108/105/108105157/

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE21 **Course Name**: Parallel Processing
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective:

- To understand the parallel processing concepts.
- To understand and analyze pipelining and software pipelining.
- To understand concepts of multithread, multiprocessing.

Course Description:

The training course is intended for mastering knowledge and skills necessary for successful start of professional activity in the domain of parallel processing. A distinctive feature of the training course is its integrity. The course provides necessary theoretical knowledge in the domain of parallel calculations and practical skills in development of parallel programs.

Course Contents:

Unit 1

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

Unit 2

Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

Unit 3

VLIW processors, Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

Unit 4

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

Unit 5

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

Unit 6

Operating systems for multiprocessors systems customizing applications on parallel processing platforms

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- Identify limitations of different architectures of computer
- Analysis quantitatively the performance parameters for different architectures
- Investigate issues related to compilers and instruction set based on type of architectures.

Text books:

- Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition

- Kai Hwang, “Advanced Computer Architecture”, TMH

Reference books:

- V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.
- William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition
- Kai Hwang, Zhiwei Xu, “Scalable Parallel Computing”, MGH
- David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.

Online links for study & reference materials:

https://nptel.ac.in/courses/117/106/117106086/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code : VPE22 **Course Name : System Design with Embedded Linux**
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective :

The purpose of an embedded operating system is: to insure the embedded system operates in an efficient and reliable manner by managing hardware and software resources. to provide an abstraction layer to simplify the process of developing higher layers of software. to act as a partitioning tool.

Course Description :

"Introduction," gives a brief history of embedded Linux and what the benefits of embedded Linux are over other RTOSs.After that architecture of embedded Linux and comparition with traditional RTOS and microkernel architectures. "Embedded Drivers," discussed in detail such as the Serial driver, Ethernet driver, I2C subsystem, and USB gadgets. "Building and Debugging," is divided into three sections: building, debugging, and profiling. "Embedded Graphics," explains in detail a generic frame buffer driver and how to write applications using the frame buffer interface and "uClinux," explains the architecture and programming environment in uClinux.

Course Contents :

Unit 1

Inroduction: Embedded Linux Vs Desktop Linux, Embedded Linux Distributions

Unit 2

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

Unit 3

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules

Unit 4

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

Unit 5

Building and Debugging: Kernel, Root file system, Embedded Graphics

Unit 6

Case study of uClinux

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- CO1: Familiarity of the embedded Linux development model.
- CO2: Write, debug, and profile applications and drivers in embedded Linux.
- CO3: Understand and create Linux BSP for a hardware platform

Text books :

- Karim Yaghmour, "Building Embededd Linux Systems", O'Reilly & Associates
- P Raghvan, Amol Lad, SriramNeelakandan, "Embedded Linux System Design and Development", Auerbach Publications

Reference books :

- Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition, 2010.
- Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014.

Online links for study & reference materials :

https://www.esys.ir/Files/Ref_Books/Linux/esys.ir_Embedded.Linux.System.Design.and.Development.pdf

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code : VPE23 **Course Name : CAD of Digital System**
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective :

To understand the basic concepts of designing combinational and sequential circuits and the possible hazards in the design.

- To model combinational and sequential circuits using VHDL.
- To design and model digital circuits using different modelling techniques and also design Finite State Machines.
- To study various programmable logic devices like SPLDs, CPLDs and FPGA.
- To study how to implement functions in FPGAs

Course Description :

This course provides the advanced knowledge of digital design using Hardware Description Language. The course deals with fundamentals of HDL, Programmable logic devices and their design and testing of logic circuits.

Course Contents :

Unit 1:

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

Unit 2:

VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

Unit 3:

General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement, routing.

Unit 4:

Simulation – logic synthesis, verification, high level Synthesis.

Unit 5 and 6:

MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

Course Learning Outcomes(CLOs) :

At the end of this course, students will be able to

- Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
- Study of various phases of CAD, including simulation, physical design, test and verification.
- Demonstrate knowledge of computational algorithms and tools for CAD.

Text books :

- N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”.

Reference books :

- S.H. Gerez, “Algorithms for VLSI Design Automation.

Online links for study & reference materials :

https://nptel.ac.in/courses/106/106/106106089/

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: MTC01 **Course Name**: Research Methodology and IPR
Course Credit: 2 **Total Contact Hour** : 20 hr

Course Objective :

- Identify an appropriate research problem in their interesting domain
- To explain various research designs and their characteristics
- To explain the art of interpretation, art of writing research reports and presentation skills
- To explain various forms of intellectual property, its relevance and business impact in the changing global business environment

Course Description:

This course emphasizes on the fundamental of research. The student first taught about research formulation and then what are the research designs needed according to research formulation. To understand and formulate the research problem the student should be aware of the aspect of effective literature review and the sources of information.to be taken to conduct literature review. Students are exposed to application of research design through which they understand that how, when and which design is required. In concurrence with this , the analysis part will be taught. Finally concepts related to patents, trademark and copyright will be taught.

Course Content:

UNIT1: Meaning of research problem, sources of research problem, characteristics of good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation. Necessary instrumentation

UNIT2: Effective literature studies approaches, analysis, plagiarism and research ethics

UNIT3: Effective technical writing, how to write report, paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT4: Nature of Intellectual property; patents, designs, trade and copyright. Process of patenting and development: technological research, innovation, patenting, development, International Scenario; International cooperation on Intellectual Property. Procedure for grants of patents, patenting under PCT.

UNIT5: Patent Rights; Scope of Patents Rights, Licensing and transfer of technology; Patent information and databases, geographical Indications.

UNIT6: New development in IPR, Administration of patent system, New developments in IPR, IPR of Biological system, Computer software etc. Traditional knowledge case studies, IPR and IITs.

Course Learning Outcomes (CLOs):

- Understand the characteristics, objects of good research problem.
- Understand concepts of data collection, analysis

- Understand significance, effective technical writing and report
- Understand the patent rights and transfer of technology

Text books:

- Stuart Melville and Wayne Goddard,'' Research methodology: an introduction for science and engineering student''
- Wayne Goddard and Stuart Melville, '' Research Methodology: An Introduction''

Reference books:

- Ranjit Kumar, 2nd Edition,''Research Methodology: A step by step Guide for beginners''
- Halbert, '' Resisting Intellectual Property'', Taylor and Francis Ltd, 2007
- Mayali,'' Industrial Design'', McGraw Hill, 1992.

Online links for study and reference materials:

https://nptel.ac.in/courses/121/106/121106007/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: MAC04 **Course Name:** Value Education
Course Credit: 0 **Total Contact Hour:** 20hr

Course Objective:

1. To make students understand the relevance of individual values in everyday lives
2. To help students imbibe different individual values in their personality
3. To help students develop good moral values and positive character
4. To help students learn the significance of self-management and self-control

Course Description:

The course is an appropriate combination of theoretical and industry specific contents on values and works ethics aimed at developing students into professionals. The course enables students learn concepts related to values and description of different types of values like individual values, social values, organizational values, etc. The course emphasizes on significance of cultivation of individual values that are essential in a personality and lists out various individual values to be imbibed in a student preparing for professional world. The course also describes various practical aspects of value education like managing good health, self-control, science of reincarnation, religious tolerance and role of women, which are pre-requisites for good moral character and competence.

Course Contents: The course is divided into 4 broad units namely:

1. **Unit-1: Values and Self-development**, Social Values and Individual attitudes, work ethics and Indian vision of humanism, moral and non-moral valuation, standards and principles, value judgments
2. **Unit-2: Importance of cultivation of values**, sense of duty, devotion, self-reliance, confidence, concentration, truthfulness, cleanliness, honesty, humanity, power of faith, national unity, patriotism, love for nature, discipline
3. **Unit-3: Personality and Behavior Development,** soul and scientific attitude, positive thinking, integrity and discipline, punctuality, love and kindness, avoid fault thinking, freedom from anger, dignity of labour, universal brotherhood, religious tolerance, true friendship, happiness vs suffering, love for truth, aware of self-destructive habits, association and cooperation, doing best for saving nature
4. **Unit-4: Character and Competence,** holy book vs blind faith, self-management and good health, science of reincarnation, equality, non-violence, humility, role of women, all religions and same message, mind yourself, self-control, honesty, studying effectively

Course Learning Outcomes (CLOs):

CLO-1: The students will be able to relate to concepts related to value education in their everyday lives.

CLO-2: The students will be able to demonstrate individual values cultivated in their respective workplaces or professional world.

CLO-3: The students will be able to differentiate between the different types of values and imbibe them as part of their self-development.

CLO-4: The students will be able to learn and practice techniques of managing good health, self-control, gender sensitivity and religious tolerance.

Text books:

1. Indrani Majhi, Ganesh Das, VALUE EDUCATION, 1, 2017, Laxmi Publications Pvt Ltd, ISBN: 9789352741120, 9352741129
2. Sharma Sandeep, Encyclopedia of Indian Ethos and Values in Management, Anmol Publications Pvt Ltd, ISBN: 9788126139187, 9788126139187

Reference books:

1. UN-HABITAT**,** Human Values And Ethics In Workplace: Improving Leadership And Performance In The Water Education, Water Supply And Sanitation Sector, 2006, United Nations Human Settlements Programme (UN-HABITAT)
2. Ganesh A. Gayatri, Values Attitude and Practices, Publisher: Discovery Publishing Pvt. Ltd, ISBN: 9789350561287, 9789350561287
3. Atkinson Camille E., Women, Ethics and the Workplace, ABC-CLIO, ISBN: 9780275960919, 9780275960919
4. Green Connie Ragen, Rethinking the Work Ethic, Hunter's Moon Publishing, ISBN: 9781937988333, 9781937988333

Online links for study & reference materials:

1. https://www.researchgate.net/publication/228079327
2. https://www.researchgate.net/publication/49586890
3. https://www.researchgate.net/publication/258040203
4. https://www.enterpreneur.com/amphtml/310254
5. https://www.ncbi.nlm.nih.gov/pmc/articles/PMC3705678

Assessment method :(Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Mid-term exam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE31 **Course Name:** Memory Technologies
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective:

- Apply their knowledge to analyze the operations of a single memory bit-cell and its related stability, variability and reliability issues.
- Understand the scaling trend of the mainstream memory technologies and the motivation for the emerging technologies.

Course Description:

In the last four decades, the number of transistors in a chip has increased from few thousands to few billions. In order to utilize the available transistors in a chip to improve computational power, various micro-architectural techniques have been proposed, which lead to the design of variety of processors, from simple in-order pipeline processors to recent multi-core processors.

Course Contents:

Unit 1

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOSSRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Unit 2

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs .SRAM and DRAM Memory controllers.

Unit 3

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit 4

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit 5

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Unit 6

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

Course Learning Outcomes (CLOs):

- Select architecture and design semiconductor memory circuits and subsystems.
- Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Knowhow of the state-of-the-art memory chip design

Text books:

- Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
- KiyooItoh, "VLSI memory chip design", Springer International Edition

Reference books:

- Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI

Online links for study & reference materials:
https://nptel.ac.in/courses/106/106/106106134/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Mid exam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code : VPE32 **Course Name : SoC Design**
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective :

In this course the students will learn SOC design processes, ASIc design flow, EDA tools, architecture design and test optimization with system integration issues

Course Description :

Students will understand the ASIC Design flow and EDA tools and also acquire knowledge about Top-down SoC design flow, Front-end and back-end chip design and will also learn interpret the design methodologies for SoC.

Course Contents :

Unit 1

ASIC:Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit 2

NISC:NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set, Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Unit 3

Simulation:Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Unit 4

Low power SoC design / Digital system, Design synergy, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5

Synthesis:Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysisSingle core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

Unit 6

Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

Course Learning Outcomes(CLOs) :

At the end of the course, students will be able to:

- Identify and formulate a given problem in the framework of SoC based design approaches
- Design SoC based system for engineering applications
- Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

Text books :

- Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
- B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

Reference books :

- RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
- P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
- Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

Online links for study & reference materials :
https://www.youtube.com/watch?v=3KLOXUYGo9s

Assessment method : (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE33 **Course Name:** Low Power VLSI
Course Credit: 3 **Total Contact Hour:** 30hr

Course Objective:

- To learn fundamentals of power dissipation in microelectronic devices.
- To identify system performance and reliability

Course Description:

This course deals with issues and models to design low-power VLSI circuits, fundamentals of power dissipation in microelectronic devices, will be able to estimate power dissipation due to switching, short circuit.

Course Contents:

Unit 1

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Unit 2

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3

Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew vs. tolerable skew, chip & package co-design of clock network.

Unit 4

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

Unit 5

Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Unit 6

Low Power Microprocessor Design System: power management support, architectural tradeoffs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

Course Learning Outcomes (CLOs) :

At the end of this course students will demonstrate the ability to

- Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- Characterize and model power consumption & understand the basic analysis methods.
- Understand leakage sources and reduction techniques.

Text books:

- Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

Reference books:

- P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002
- Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.
- J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
- A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995

Online links for study & reference materials:

https://nptel.ac.in/courses/117/101/117101004/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE41 **Course Name:** Communication Buses & Interfaces
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective:

- Explain why a parallel interface is needed in an embedded system.
- List the names of common parallel bus standards along with their important features.

Course Description:

Interfaces in the sector of system and process control include those that serve to exchange information in the form of physical (e.g. electrical voltage) or logical (data) parameters. Transmission can be either analog or digital. There are various types of interface depending on the level at which communication takes place.

Course Contents:

Unit 1

Serial Buses, Physical interface, Data and Control signals, features

Unit 2

limitations and applications of RS232, RS485, I^2C, SPI

Unit 3

CAN - Architecture, Data transmission, Layers, Frame formats, applications

Unit 4

PCIe - Revisions, Configuration space, Hardware protocols, applications

Unit 5

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

Unit 6

Data Streaming Serial Communication Protocol- Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

Course Learning Outcomes (CLOs):

- Select a particular serial bus suitable for a particular application.
- Develop APIs for configuration, reading and writing data onto serial bus.
- Design and develop peripherals that can be interfaced to desired serial bus.

Text books:

- Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ", Lakeview Research, 2nd Edition.
- Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press.

Reference books:

- Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.

Online links for study & reference materials:
https://nptel.ac.in/courses/108/103/108103157/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%

Assessment-3(Mid exam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE42 **Course Name:** Network Security and Cryptography
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective:

- To know about various encryption techniques.
- To understand the concept of Public key cryptography.
- To study about message authentication and hash functions
- To impart knowledge on Network security

Course Description:

The aim of this course is to introduce the student to the areas of cryptography and cryptanalysis. This course develops a basic understanding of the algorithms used to protect users online and to understand some of the design choices behind these algorithms. Our aim is to develop a workable knowledge of the mathematics used in cryptology in this course.

Course Contents:

Unit 1

Security- Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Unit 2

Number Theory- Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit 3

Private-Key (Symmetric) Cryptography- Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES),Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit 4

Public-Key (Asymmetric) Cryptography- RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms:MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Unit 5

Authentication- IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Unit 6

System Security- Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

Course Learning Outcomes (CLOs):

- Identify and utilize different forms of cryptography techniques.
- Incorporate authentication and security in the network applications.
- Distinguish among different types of threats to the system and handle the same.

Text books:

- William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
- Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition

Reference books:

- Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

Online links for study & reference materials :
https://nptel.ac.in/courses/106/105/106105162/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Mid exam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE43 **Course Name:** Physical Design Automation
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective:

- Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods

Course Description:

The course will introduce the participants to the basic design flow in VLSI physical design automation, the basic data structures and algorithms used for implementing the same. The course will also provide examples and assignments to help the participants to understand the concepts involved, and appreciate the main challenges therein.

Course Contents:

Unit 1: Introduction to VLSI Physical Design Automation.
Unit 2: Standard cell, Performance issues in circuit layout, delay models Layout styles.
Unit 3: Discrete methods in global placement.
Unit 4: Timing-driven placement. Global Routing Via Minimization.
Unit 5: Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.
Unit 6: Compaction, algorithms, Physical Design Automation of FPGAs..

Course Learning Outcomes(CLOs) :

At the end of the course, students will be able to:

- Study automation process for VLSI System design.
- Understanding of fundamentals for various physical design CAD tools.
- Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

Text books:

- S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley ,1998.
- N.A.Sherwani , "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer,1999.

Reference books:

- S.M. Sait , H. Youssef, "VLSI Physical Design Automation", World scientific, 1999.
- M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.

Online links for study & reference materials:

https://nptel.ac.in/courses/106/105/106105161/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE51 **Course Name: Communication Networks**
Course Credit: 03 **Total Contact Hour:** 40hr

Course Objective:

- To develop an understanding of computer networking basics.
- To develop an understanding of different components of computer networks, various protocols, modern technologies and their applications.

Course Description:

This course provides an introduction to computer networks, with a special focus on the Internet architecture and protocols. Topics include layered network architectures, addressing, naming, forwarding, routing, communication reliability, the client-server model, web and email protocols. Besides the theoretical foundations, students acquire practical experience by programming reduced versions of real Internet protocols.

Course Contents:

Unit 1: Introduction:- Network Architecture, Performance
Unit 2: Connecting nodes:- Connecting links, Encoding, framing, Reliable transmission, Ethernet and Multiple access networks, Wireless networks
Unit 3: Queuing models- For a) one or more servers b) with infinite and finite queue size c) Infinite population.Internetworking:- Switching and bridging, IPv4, Addressing, Routing Protocols, Scale issues, Routers - Architecture, IPv6
Unit 4: End-to-End Protocols:- Services, Multiplexing, De-multiplexing, UDP, TCP, RPC, RTP
Unit 5: Congestion control and Resource Allocation- Issues, Queuing disciplines, TCP congestion control, Congestion Avoidance, QoS Applications:- Domain Name Resolution, File Transfer, Electronic Mail, WWW, Multimedia Applications
Unit 6: Network monitoring – Packet sniffing tools such as Wireshark Simulations using NS2/OPNET

Course Outcomes:

At the end of the course, students will be able to:

- Analyze protocols and algorithms, acknowledge tradeoffs and rationale
- Use routing, transport protocols for the given networking scenario and application
- Evaluate and develop small network applications

Text books:

1. Larry L. Peterson, Bruce S, Devie, “Computer Networks” , MK, 5th Edition
2. Aaron Kershenbaum, “Telecommunication Network Design Algorithms”, MGH, International Edition 1993.

Reference books:

1. Vijay Ahuja, “Communications Network Design and Analysis of Computer Communication Networks”, MGH, International Editions.
2. Douglas E. Comer, “Internetworking with TCP/IP”, Pearson Education, 6th Edition

Online links for study & reference materials:

https://nptel.ac.in/courses/106/105/106105183/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code:VPE52 **Course Name:** Selected Topics in Mathematics
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective:

- To understand Probability and Statistics
- To analyze Special Distributions, Joint Distributions
- To understand characteristics Multivariate Data Analysis
- To understand concepts of tress and graph.

Course Description:

This course emphasizes on the profanity and other mathematical and statistical concepts. These concepts are necessary and helpful in designing devices and circuits and studying their behavior.

Course Contents:

Unit 1:

Probability and Statistics:- Definitions, conditional probability, Bayes Theorem and independence.

- Random Variables: Discrete, continuous and mixed random variables, probability mass, Probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

Unit 2:

Special Distributions: Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions.- Pseudo random sequence generation with given distribution, Functions of a Random Variable

Unit 3:

Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.

- Stochastic Processes: Definition and classification of stochastic processes, Poisson process
- Norms, Statistical methods for ranking data

Unit 4:

Multivariate Data Analysis- Linear and non-linear models, Regression, Prediction and Estimation

- Design of Experiments – factorial method
- Response surface method

Unit 5:

Graphs and Trees:- Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring

Unit 6:

Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set, theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning tree

Course Learning Outcomes(CLOs) :

At the end of the course, students will be able to:

- Characterize and represent data collected from experiments using statistical methods.
- Model physical process/systems with multiple variables towards parameter estimation and prediction
- Represent systems/architectures using graphs and trees towards optimizing desired objective.

Text books:

- Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rd Edition
- C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2nd Edition

Reference books:

- Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons, 2001.
- Douglas C. Montgomery, "Design and Analysis of Experiments", John Wiley and Sons, 2001.
- B. A. Ogunnaike, "Random Phenomena: Fundamentals of Probability and Statistics for Engineers", CRC Press, 2010.

Online links for study & reference materials:

https://nptel.ac.in/courses/115/106/115106086/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Course Code: VPE53 **Course Name:** Nano materials and Nanotechnology
Course Credit: 3 **Total Contact Hour:** 40hr

Course Objective:

- To foundational knowledge of the Nanoscience and related fields.
- To make the students acquire an understanding the Nanoscience and Applications
- To help them understand in broad outline of Nanoscience and Nanotechnology.

Course Description:

This course aims to cover a number of topics in nanotechnology and science, with emphasis on the characteristics of Nanomaterials (role of size, mechanical, photovoltaic, thermal, classification of Nanomaterials, relationship between properties and composition of Nanomaterials, etc.) (Solar, chemical vapor deposition, plasma-RF, ionic excitation, laser etching, electrophoresis, etc.); nanoscale characterization instruments (XRD, SEM, TEM, Nanoparticles, etc.).

Course Contents:

Unit 1: Nanomaterials in one and higher dimensions,
Unit 2: Applications of one and higher dimension nano-materials.
Unit 3: Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics.
Unit 4: Carbon nanotubes – synthesis and applications
Unit 5 and 6: Interdisciplinary arena of nanotechnology.

Course Learning Outcomes(CLOs) :

At the end of the course, students will be able to:

- To understand the basic science behind the design and fabrication of nano scale systems.
- To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
- To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
- To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

Text books:

- Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards, 2nd edn, John Wiley and Sons, 2009.
- Nanocrystalline Materials by A I Gusev and A ARempel, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.

Reference books:

- Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn, 2010.
- Carbon Nanotubes: Synthesis, Characterization and Applications by Kamal K. Kar, Research Publishing Services; 1stedn, 2011, ISBN-13: 978-9810863975.

Online links for study & reference materials:

https://nptel.ac.in/courses/117/106/117106086/

Assessment method: (Continuous Internal Assessment = 40% , Final Examination = 60%)

Assessment -1	- 05%
Assessment-2	- 05%
Assessment-3(Midexam)	- 20%
Assessment-3	- 05%
Assessment-4	- 05%
Total Internal Assessment	**- 40%**

Dissertation

Dissertation Phase – I and Phase - II

Teaching Scheme **Paper Code: MTC03 & MTC04**

Lab work: 20 and 32 hrs/week

Course Outcomes:

At the end of this course, students will be able to

- Ability to synthesize knowledge and skills previously gained and applied to an in depth study and execution of new technical problem.
- Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design.
- Ability to present the findings of their technical solution in a written report.
- Presenting the work in International/ National conference or reputed journals.

Syllabus Contents:

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.

Guidelines for Dissertation Phase – I and II:

- As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
- The dissertation may be carried out preferably in-house i.e. departments laboratories and centers OR in industry allotted through departments T & P coordinator.

- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/ Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.